CLAIMS

What is claimed is:

1. A multi-layered interconnect structure adapted for electrically interconnecting a semiconductor chip and a circuitized substrate using solder connections, said interconnect structure comprising:

a thermally conductive layer including first and second opposing surfaces;

first and second dielectric layers positioned on said first and second opposing surfaces, respectively; and

first and second pluralities of electrically conductive members positioned on said first and second dielectric layers, respectively, each of said first and second pluralities of said electrically conductive members adapted for having solder connections thereon, for being electrically connected to a semiconductor chip and a circuitized substrate, respectively, said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip and between said second plurality of electrically conductive members and said circuitized substrate.

2. The multi-layered interconnect structure of claim 1 wherein said thermally conductive layer comprises a metal layer.

3. The multi-layered interconnect structure of claim 2 wherein said metal is selected from the group consisting of nickel, copper, molybdenum, and iron.

4. The multi-layered interconnect structure of claim 3 wherein said nickel comprises from about 38% to about 44% of said metal.

5. The multi-layered interconnect structure of claim 3 wherein said iron comprises from about 56% to about 62% of said metal.

6. The multi-layered interconnect structure of claim 2 wherein said metal layer is comprised of a layer of nickel and iron having a copper layer with a first thickness positioned thereon.

7. The multi-layered interconnect structure of claim 6 wherein said first thickness of said copper layer comprises from about 10% to about 14 % of said thickness of said material of said thermally conductive layer.

8. The multi-layered interconnect structure of claim 1 wherein said thickness of said material of said thermally conductive layer is from about 1.0 to about 3.0 mils.

9. The multi-layered interconnect structure of claim 1 wherein said coefficient of thermal expansion of said material of said thermally conductive layer is from about 4.0 to about 8.0 ppm/degree C.

10. The multi-layered interconnect structure of claim 1 wherein said first and second dielectric layers are each comprised of a layer of non-cloth dielectric material.

11. The multi-layered interconnect structure of claim 10 wherein said non-cloth dielectric material comprises polytetrafluoroethylene having a filler material therein.

12. The multi-layered interconnect structure of claim 11 wherein said filler material is silica.

13. The multi-layered interconnect structure of claim 1 wherein each of said first and second dielectric layers have a thickness from about 1.0 to about 9.0 mils.

14. The multi-layered interconnect structure of claim 1 wherein at least one of said first and second dielectric layers includes a layer having an effective modulus to assure sufficient compliancy of said interconnect structure during operation.

15. The multi-layered interconnect structure of claim 14 wherein said effective modulus is from about 0.01 to about 0.50 Mpsi.

16. The multi-layered interconnect structure of claim 1 wherein said first and second pluralities of electrically conductive members are comprised of copper.

17. The multi-layered interconnect structure of claim 1 wherein selected ones of said first plurality of electrically conductive members each include a thickness of from about 0.25 to about 1.5 mils.

18. The multi-layered interconnect structure of claim 1 wherein selected ones of said second plurality of electrically conductive members each include a thickness of from about 0.25 to about 1.5 mils.

19. The multi-layered interconnect structure of claim 1 further including a first electrically conductive layer within said first dielectric layer.

20. The multi-layered interconnect structure of claim 19 further including a second electrically conductive layer within said first dielectric layer and positioned between said first electrically conductive layer and said thermally conductive layer.

21. The multi-layered interconnect structure of claim 20 wherein each of said first and second electrically conductive layers has a thickness from about 0.20 to about 1.0 mils.

22. The multi-layered interconnect structure of claim 20 wherein said first and second electrically conductive layers are comprised of a metal selected from the group consisting of copper or aluminium.

23. The multi-layered interconnect structure of claim 20 wherein said second electrically conductive layer comprises a first plurality of shielded signal conductors.

24. The invention of claim 23 wherein said multi-layered interconnect structure further includes a first plated through hole adapted for being positioned under said semiconductor chip, said first plated through hole electrically connected to at least one electrically conductive member of said first plurality of electrically conductive members, to at least one of said first plurality of shielded signal conductors and to at least one electrically conductive member of said second plurality of electrically conductive members.

25. The multi-layered interconnect structure of claim 24 further including a third dielectric layer positioned on said first dielectric layer and on portions of said first plurality of electrically conductive members, said third dielectric layer substantially overlying said first plated through hole.

26. The multi-layered interconnect structure of claim 25 wherein said third dielectric layer comprises a layer of laser ablatable dielectric material.

27. The multi-layered interconnect structure of claim 26 wherein said third dielectric includes an internal wall defining an opening therein, said opening exposing at least a portion of at least one of said first plurality of electrically conductive members, said internal wall including a conductive layer thereon.

28. The multi-layered interconnect structure of claim 27 wherein said conductive layer on said internal wall of said opening is also positioned on said exposed portion of said at least one of said first plurality of electrically conductive members.

29. The multi-layered interconnect structure of claim 28 wherein said conductive layer on said internal wall of said opening and on said exposed portion of said at least one of said first plurality of electrically conductive members defines a first microvia.

30. The multi-layered interconnect structure of claim 29 wherein said first microvia is electrically connected to said first plated through hole.

31. The multi-layered interconnect structure of claim 1 further including a third electrically conductive layer within said second dielectric layer.

32. The multi-layered interconnect structure of claim 31 further including a fourth electrically conductive layer within said second dielectric layer and positioned between said third electrically conductive layer and said thermally conductive layer.

33. The multi-layered interconnect structure of claim 32 wherein each of said third and fourth electrically conductive layers has a thickness from about 0.20 to about 1.0 mils.

34. The multi-layered interconnect structure of claim 32 wherein said third and fourth electrically conductive layers are each comprised of a metal selected from the group consisting of copper and aluminium.

35. The multi-layered interconnect structure of claim 32 wherein said fourth electrically conductive layer comprises a second plurality of shielded signal conductors.

36. The invention of claim 35 wherein said multi-layered interconnect structure further includes a second plated through hole adapted for being positioned under said semiconductor chip, said second plated through hole electrically connected to at least one electrically conductive member of said first plurality of electrically conductive members, to at least one of said second plurality of shielded signal conductors and to at least one electrically conductive member of said second plurality of electrically conductive members.

37. The multi-layered interconnect structure of claim 36 further including a fourth dielectric layer positioned on said second dielectric layer and on portions of said second plurality of electrically conductive members, said fourth dielectric layer substantially overlying said second plated through hole.

38. The multi-layered interconnect structure of claim 37 wherein said fourth dielectric layer comprises a layer of laser ablatable dielectric material.

39. The multi-layered interconnect structure of claim 38 wherein said fourth dielectric layer incudes an internal wall defining an opening therein, said openings exposing at least a portion of at least one of said second plurality of electrically conductive members, said internal wall including a conductive layer thereon.

40. The multi-layered interconnect structure of claim 39 wherein said conductive layer on said internal wall of said opening within said fourth dielectric layer is also positioned on said exposed portion of said at least one of said second plurality of electrically conductive members.

41. The multi-layered interconnect structure of claim 40 wherein said conductive layer on said internal wall of said opening within said fourth dielectric layer and on said exposed portion of said second plurality of electrically conductive members defines a second microvia.

42. An electronic package comprising:

a semiconductor chip having a first surface, said first surface including a plurality of contact members; and

an multi-layered interconnect structure adapted for electrically interconnecting said semiconductor chip to a circuitized substrate, said multi-layered interconnect structure including a thermally conductive layer having first and second opposing surfaces, first and second dielectric layers positioned on said first and second opposing surfaces, respectively, and first and second pluralities of electrically conductive members positioned on said first and second dielectric layers, respectively, said first plurality of electrically conductive members having a plurality of solder connections electrically connected thereto, respective ones of said solder connections being electrically connected to respective ones of said plurality of contact members on said semiconductor chip, said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip.

43. The electronic package of claim 42 wherein said contact members comprise C4 connections.

44. The electronic package of claim 43 wherein at least one of said first and second dielectric layers includes a layer having an effective modulus to assure sufficient compliancy of said multi-layered interconnect structure during operation.

45. The electronic package of claim 44 wherein said effective modulus is from about 0.01 to about 0.50 Mpsi.

46. The electronic package of claim 42 further including a first electrically conductive layer within said first dielectric layer.

47. The electronic package of claim 46 further including a second electrically conductive layer within said first dielectric layer and positioned between said first electrically conductive layer and said thermally conductive layer.

48. The electronic package of claim 47 wherein said second electrically conductive layer comprises a first plurality of shielded signal conductors.

49. The invention of claim 48 wherein said multi-layered interconnect structure further includes a first plated through hole adapted for being positioned under said semiconductor chip, said first plated through hole electrically connected to at least one electrically conductive member of said first plurality of electrically conductive members, to at least one of said first plurality of shielded signal conductors and to at least one electrically conductive member of said second plurality of electrically conductive members.

50. The electronic package of claim 49 further including a third dielectric layer positioned on said first dielectric layer and on portions of said first plurality of electrically conductive members, said third dielectric layer substantially overlying said first plated through hole.

51. The electronic package of claim 50 wherein said third dielectric layer comprises a layer of laser ablatable dielectric material.

52. The electronic package of claim 51 wherein said third dielectric includes an internal wall defining an opening therein, said opening exposing at least a portion of at least one of said first plurality of electrically conductive members, said internal wall including a conductive layer thereon.

53. The electronic package of claim 52 wherein said conductive layer on said internal wall of said opening is also positioned on said exposed portion of said at least one of said first plurality of electrically conductive members.

54. The electronic package of claim 53 wherein said conductive layer on said internal wall of said opening and on said exposed portion of said at least one of said first plurality of electrically conductive members defines a first microvia.

55. The electronic package of claim 54 wherein said first microvia is electrically connected to said first plated through hole.

56. The electronic package of claim 42 wherein said plurality of solder connections includes a layer of eutectic solder material positioned on said first microvia.

57. The electronic package of claim 42 further including a third electrically conductive layer within said second dielectric layer.

58. The electronic package of claim 57 further including a fourth electrically conductive layer within said second dielectric layer and positioned between said third electrically conductive layer and said thermally conductive layer.

59. The electronic package of claim 58 wherein said fourth electrically conductive layer comprises a second plurality of shielded signal conductors.

60. The invention of claim 59 wherein said multi-layered interconnect structure further includes a second plated through hole adapted for being positioned under said semiconductor chip, said second plated through hole electrically connected to at least one electrically conductive member of said first plurality of electrically conductive members, to at least one of said second plurality of shielded signal conductors and to at least one electrically conductive member of said second plurality of electrically conductive members.

61. The electronic package of claim 60 further including a fourth dielectric layer positioned on said second dielectric layer and on portions of said second plurality of electrically conductive members, said fourth dielectric layer substantially overlying said second plated through hole.

62. The electronic package of claim 61 wherein said fourth dielectric layer comprises a layer of laser ablatable dielectric material.

63. The electronic package of claim 62 wherein said fourth dielectric layer includes an internal wall defining an opening therein, said openings exposing at least a portion of at least one of said second plurality of electrically conductive members, said internal wall including a conductive layer thereon.

64. The electronic package of claim 63 wherein said conductive layer on said internal wall of said opening within said fourth dielectric layer is also positioned on said exposed portion of said at least one of said second plurality of electrically conductive members.

65. The electronic package of claim 62 wherein said conductive layer on said internal wall of said opening within said fourth dielectric layer and on said exposed portion of said at least one of said second plurality of electrically conductive members defines a second microvia.

66. The electronic package of claim 42 further including said circuitized substrate, said circuitized substrate having a first surface including a plurality of contact pads thereon, said second plurality of electrically conductive members of said multi-layered interconnect structure including a second plurality of solder connections electrically connected thereto, respective ones of said second plurality of said solder connections being electrically connected to respective ones of said plurality of said contact pads on said circuitized substrate.

67. The electronic package of claim 66 wherein said second plurality of said solder connections are solder balls and/or solder columns.

68. The electronic package of claim 66 wherein said solder comprises eutectic solder.

69. A method of making a multi-layered interconnect structure adapted for electrically interconnecting a semiconductor chip and a circuitized substrate using solder connections, said method comprising the steps of:

providing a thermally conductive layer including first and second opposing surfaces;

positioning first and second dielectric layers on said first and second opposing surfaces of said thermally conductive layer, respectively; and

positioning first and second pluralities of electrically conductive members on said first and second dielectric layers, respectively, each of said first and second pluralities of said electrically conductive members adapted for having solder connections thereon for being electrically connected to a semiconductor chip and a circuitized substrate, respectively, said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip and between said second plurality of electrically conductive members and said circuitized substrate.

70. The method of making the multi-layered interconnect structure of claim 69 wherein said step of positioning said first and second dielectric layers on said first and second opposing surfaces of said thermally conductive layer, respectively, comprises laminating said first and second dielectric layers onto said first and second opposing surfaces at a pressure of from about 1000 to about 2000 psi and at a temperature of from about 600 to about 750 ° F.

71. The method of making the multi-layered interconnect structure of claim 69 wherein said positioning said first and second pluralities of electrically conductive members on said first and second dielectric layers, respectively, comprises the steps of:

laminating a copper foil onto said first and second dielectric layers; and

etching selected portions of said copper foil to produce first and second pluralities of said electrically conductive members.

72. The method of making the multi-layered interconnect structure of claim 69 further including the steps of:

positioning a third dielectric layer on said first dielectric layer and on said first plurality of electrically conductive members;

removing portions of said third dielectric layer to expose portions of said first plurality of electrically conductive members; and

forming a first plurality of microvias within said third dielectric layer to expose at least a portion of at least one of said first plurality of electrically conductive members.

73. The method of making the multi-layered interconnect structure of claim 72 wherein said removing of said portions of said third dielectric layer is performed by laser ablating.

74. The method of making the multi-layered interconnect structure of claim 69 further including the steps of:

positioning a fourth dielectric layer on said second dielectric layer and on said second plurality of electrically conductive members;

removing portions of said fourth dielectric layer to expose portions of said second plurality of electrically conductive members; and

forming a second plurality of microvias within said fourth dielectric layer to expose at least a portion of at least one of said second plurality of electrically conductive members.

75. The method of making the multi-layered interconnect structure of claim 74 wherein the step of removing portions of said fourth dielectric layer is performed by laser ablating.

76. A method of making an electronic package comprising the steps of:

providing a semiconductor chip having a first surface including a plurality of contact members thereon;

providing a multi-layered interconnect structure adapted for electrically interconnecting said semiconductor chip to a circuitized substrate, said multi-layered interconnect structure including a thermally conductive layer, having first and second opposing surfaces, first and second dielectric layers positioned on said first and second opposing surfaces, respectively, and first and second pluralities of electrically conductive members positioned on said first and second dielectric layers, respectively;

providing a first plurality of solder connections on said first plurality of electrically conductive members; and

connecting respective ones of said first plurality of solder connections to respective ones of said plurality of contact members on said semiconductor chip, said thermally conductive layer being comprised of a material having a selected thickness and coefficient of thermal expansion to substantially prevent failure of said solder connections between said first plurality of electrically conductive members and said semiconductor chip.

77. The method of making the electronic package of claim 76 wherein said step of providing said first plurality of solder connections on said first plurality of electrically conductive members includes:

forming a plurality of openings in said third dielectric layer, each of said openings including an internal wall and exposing a portion of at least one of said first plurality of electrically conductive members;

plating a conductive layer on said internal wall of said plurality of openings and on said exposed portion of said at least one of said first plurality of electrically conductive members to define a plurality of microvias;

applying a first solder paste onto said conductive layer; and

reflowing said first solder paste to form a first plurality of solder connections..

78. The method of making the electronic package of claim 77 wherein said step of connecting respective ones of said first plurality of solder connections to respective ones of said plurality of contact members on said semiconductor chip further includes the steps of applying a second solder paste onto said respective ones of said first plurality of solder connections, positioning said respective ones of said contact members of said semiconductor chip against said respective ones of said first plurality of solder connections, and reflowing said second solder paste and said respective ones of said first plurality of solder connections to electrically connect said semiconductor chip to said multi-layered interconnect structure.

79. The method of making the electronic package of claim 76 further including the steps of:

providing a circuitized substrate having a first surface including a plurality of contact pads thereon;

providing a second plurality of solder connections on said second plurality of conductive members of said multi-layered interconnect structure; and

connecting respective ones of said second plurality of said solder connections to respective ones of said plurality of contact pads on said circuitized substrate to make electrical connections therebetween.